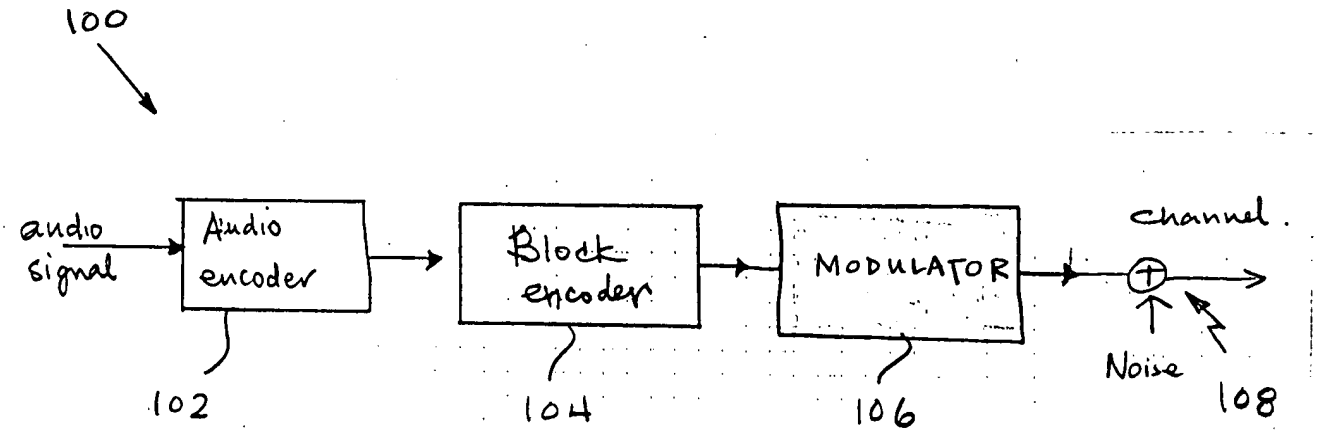

FIG. 1
(PRIOR ART)

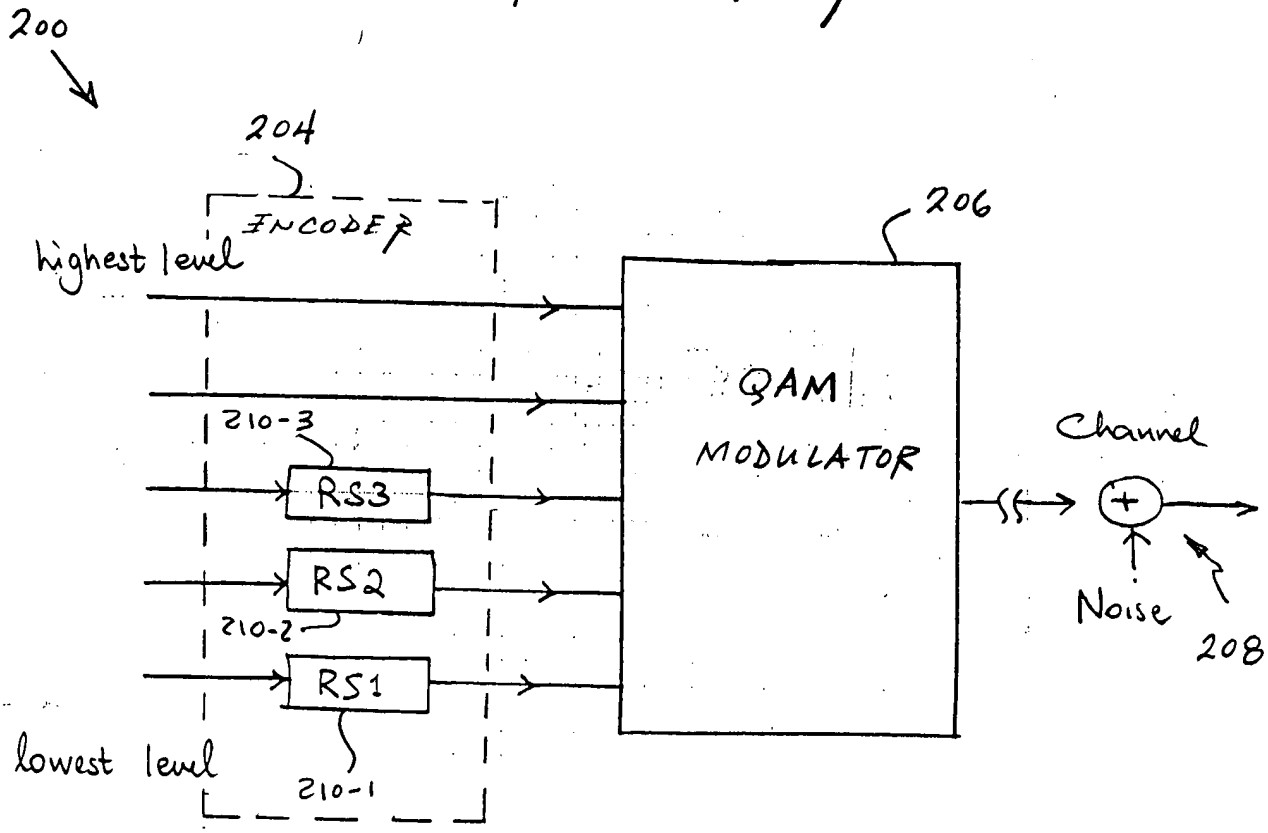

FIG. 2

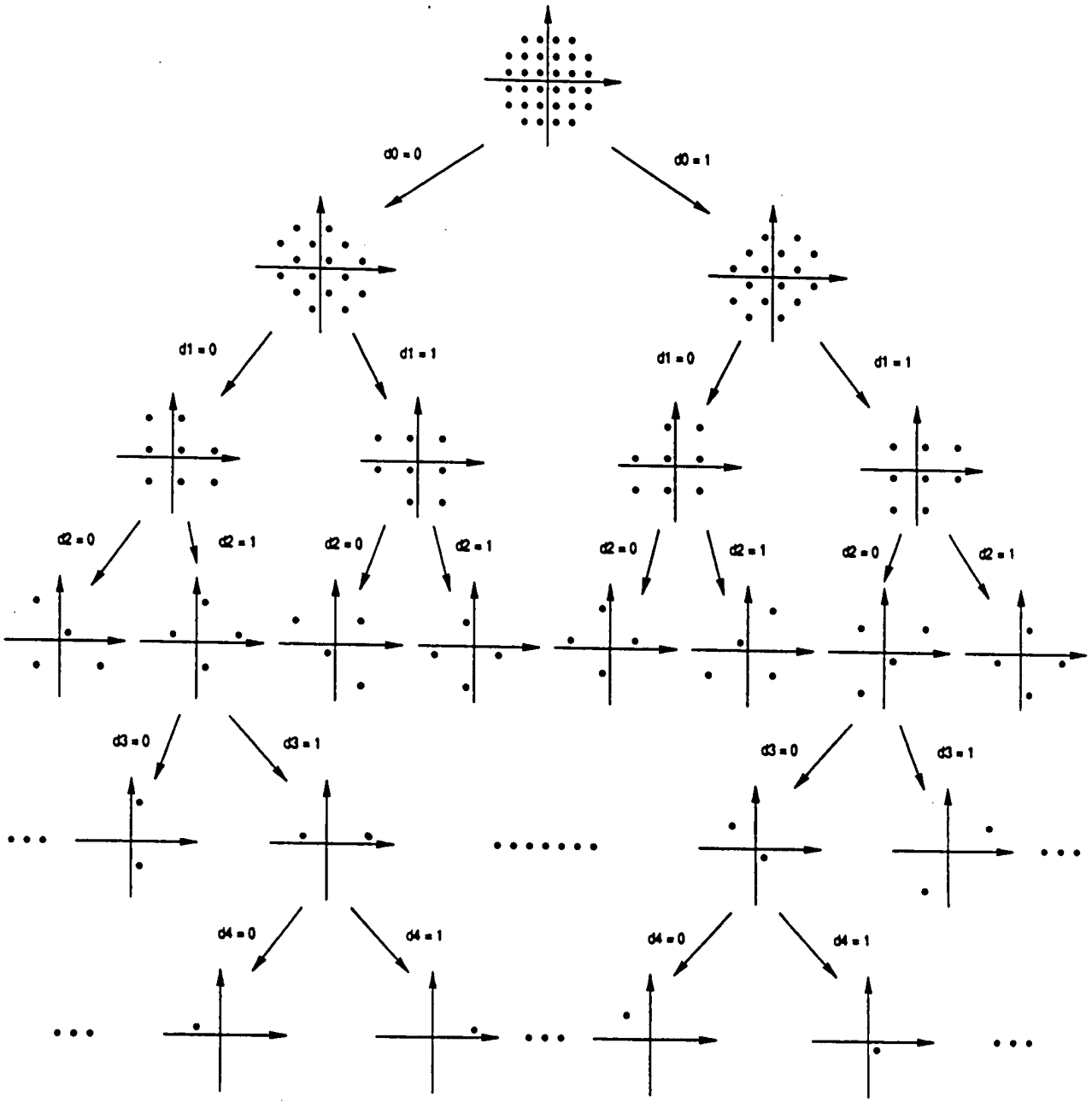
d0 = 0
d0 = 1
d1 = 0
d1 = 1
d1 = 0
d1 = 1
d2 = 0
d2 = 1
d2 = 0
d2 = 1
d2 = 0
d2 = 1
d2 = 0
d2 = 1
d3 = 0
d3 = 1
d3 = 0
d3 = 1
d4 = 0
d4 = 1
d4 = 0
d4 = 1

FIG. 3

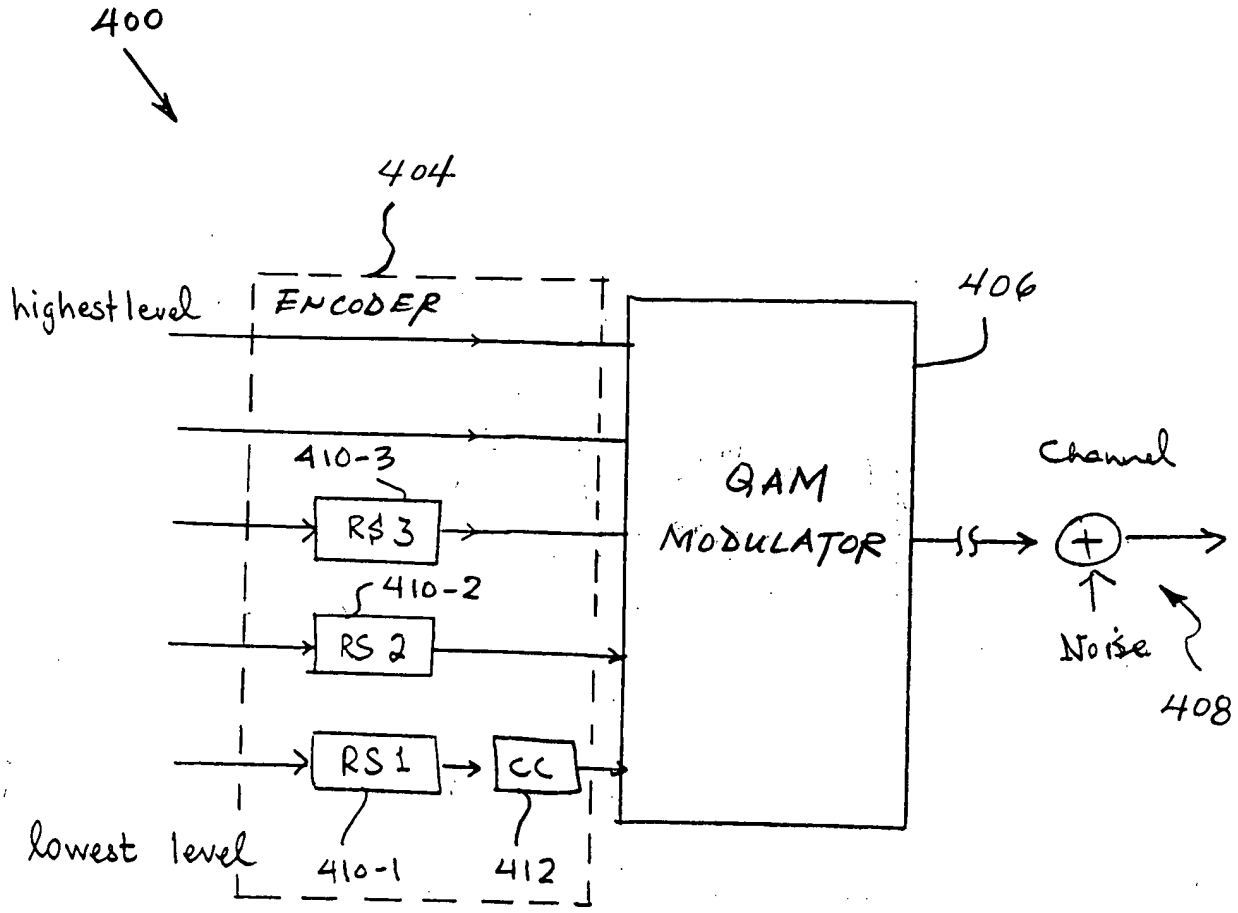
400
404
highest level
ENCODER
406
410-3
RS 3
QAM
MODULATOR
Channel
410-2
RS 2
Noise
408
RS 1
CC
lowest level
410-1
412

FIG. 4

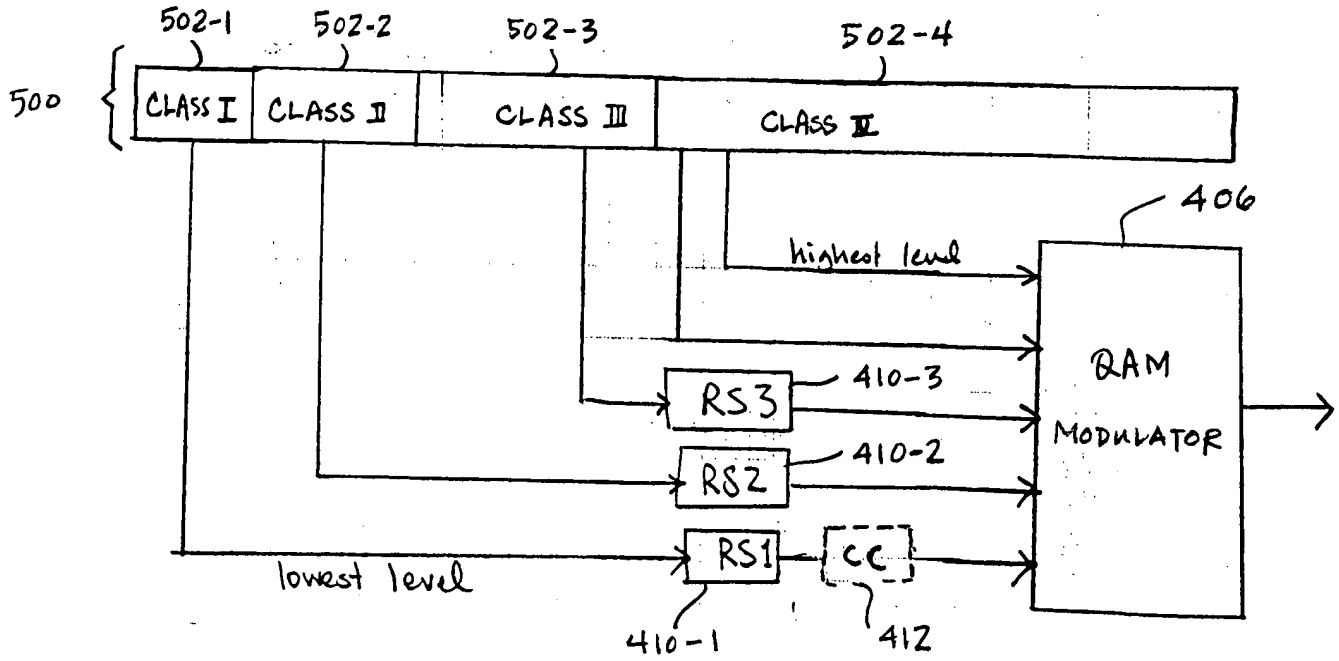
502-1
502-2
502-3
502-4
500
CLASS I
CLASS II
CLASS III
CLASS IV
406
highest level
RAM
MODULATOR
RS3
410-3
RS2
410-2
RS1
CC
lowest level
410-1
412

FIG. 5

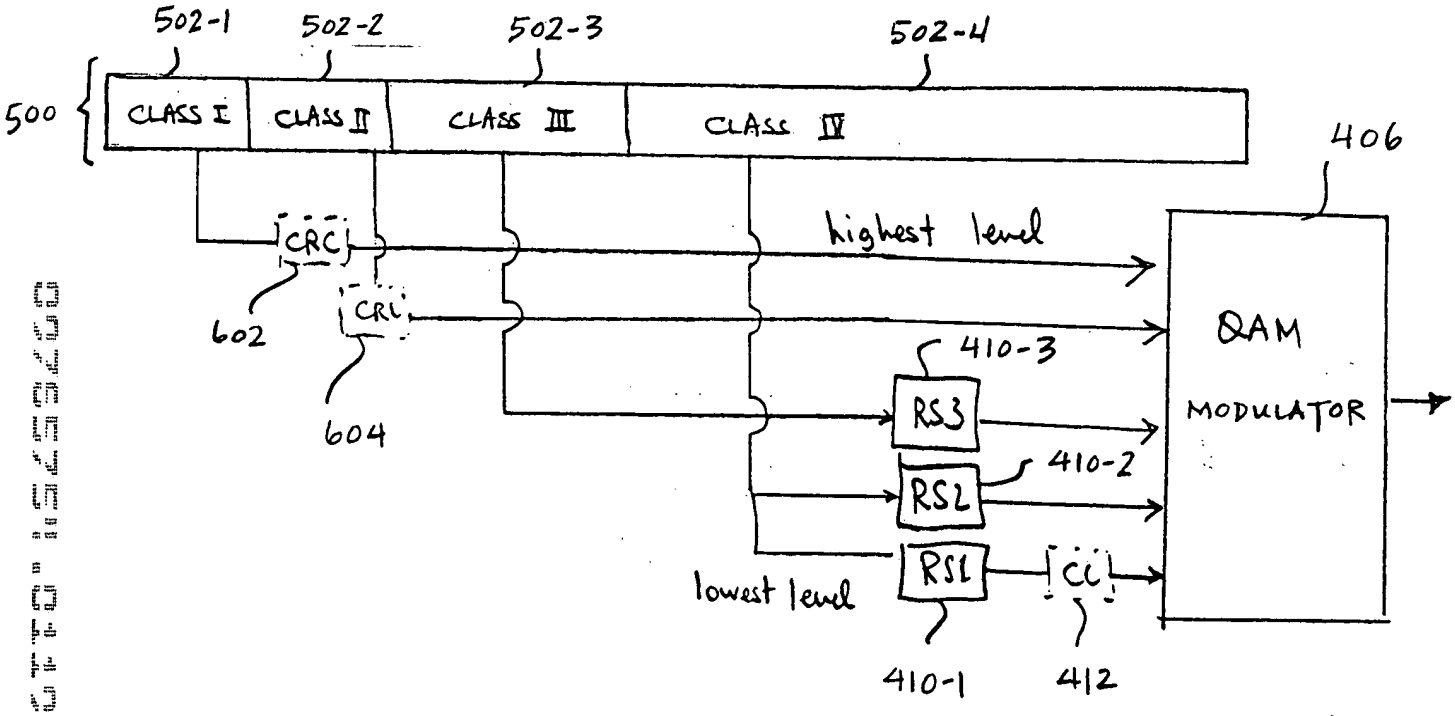
502-1
502-2
502-3
502-4
500
CLASS I
CLASS II
CLASS III
CLASS IV
406
CRC
602
CRC
604
highest level
QAM
MODULATOR
410-3
RS3
410-2
RS2
RS1
lowest level
CC
410-1
412

FIG. 6

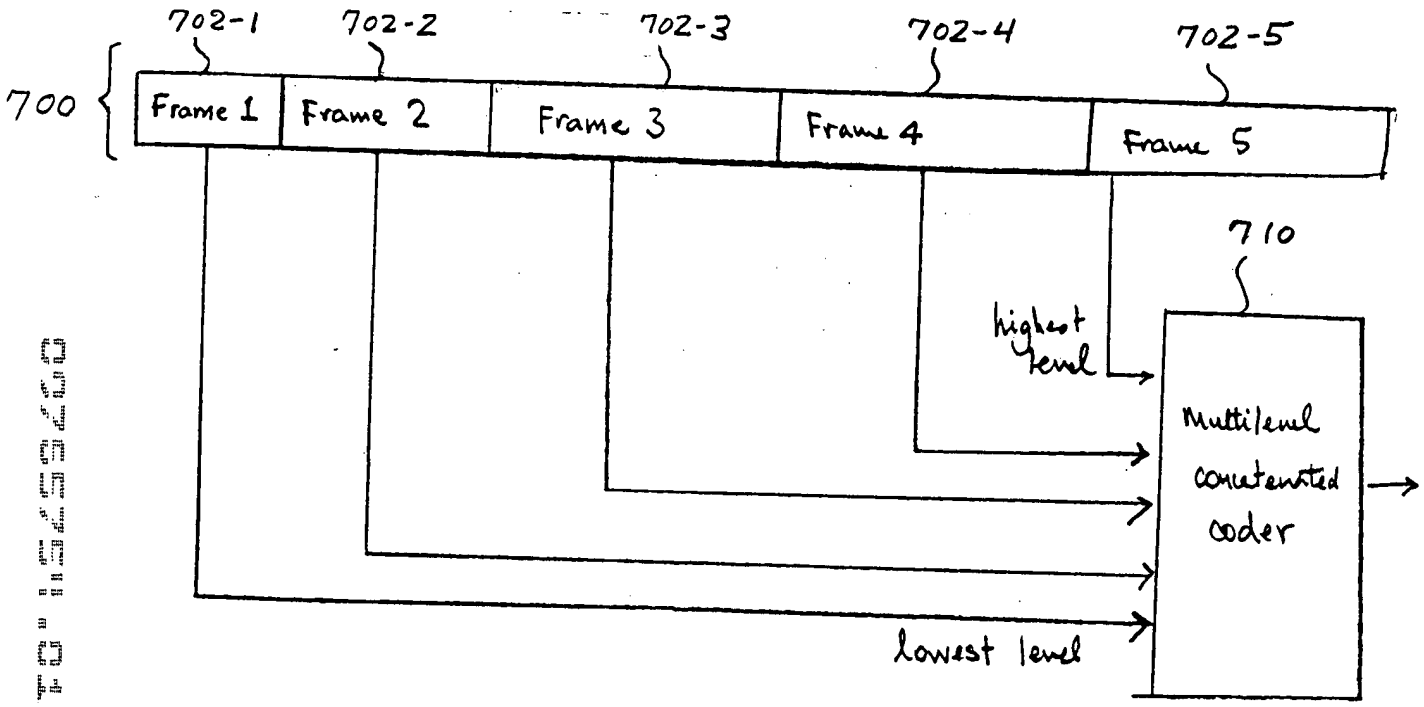
700
702-1
702-2
702-3
702-4
702-5
Frame 1
Frame 2
Frame 3
Frame 4
Frame 5
710
highest level
Multilevel concatenated coder
lowest level

FIG. 7

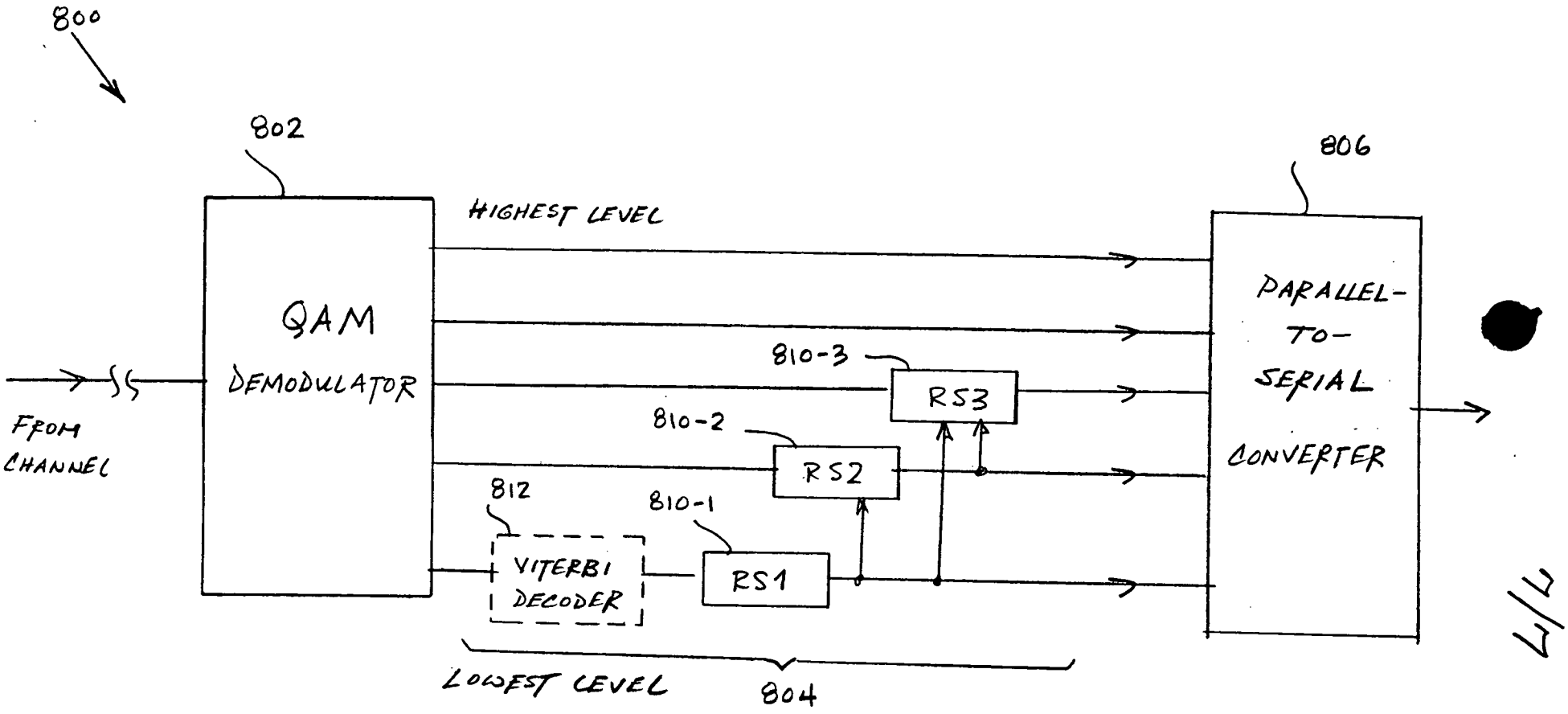
800
802
806
HIGHEST LEVEL
QAM
DEMODULATOR
FROM
CHANNEL
810-3
RS3
810-2
RS2
812
810-1
VITERBI
DECODER
RS1
PARALLEL-
TO-
SERIAL
CONVERTER
LOWEST LEVEL
804

FIG. 8